REMARKS

This Amendment is in response to the Office Action dated December 23, 2004. In the Office Action, the Examiner rejected claims 1-24 under 35 U.S.C. § 103(a) as being unpatentable over Furner *et al.*, U.S. Patent No. 5,974,474 (hereinafter *Furner*), in view of Dinallo, U.S. Patent No. 5,727,212 (hereinafter *Dinallo*).

Claims 1, 9, 19, 21, and 24 are amended as shown above. Specifically, independent claims 1, 9, and 19 are amended to more clearly recite features of the claimed invention. Further, claims 19 and 21 are amended to clarify that these claims do not fall within 35 U.S.C. § 112, second paragraph. Additionally, claims 1 and 9 have been amended to clearly recite statutory subject matter as defined by 35 U.S.C. § 101. For the reasons set forth below, the Applicants respectfully request reconsideration and allowance of all pending claims.

Argument in Support of Allowance of Claims over Claim Rejections under 35 U.S.C. § 103

To establish a *prima facie* case of obviousness, there must first be some suggestion or motivation to modify a reference or to combine references, and second be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. M.P.E.P. § 706.02(j) from *In Re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Where claimed subject matter has been rejected as obvious in view of a combination of prior art references, a proper analysis under § 103 requires, *inter alia*, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed device; and (2) whether the prior art would also have revealed that in so making, those of ordinary skill would have a reasonable expectation of success. Both the suggestion and the reasonable expectation of

success must be founded in the prior art, not in the Applicants' disclosure. *Amgen v. Chugai Pharmaceutical*, 927 F.2d 1200, 18 USPQ2d 1016 (Fed. Cir. 1991), *Fritsch v. Lin*, 21 USPQ2d 1731 (Bd. Pat. App. & Int'f 1991). An invention is non-obvious if the references fail not only to expressly disclose the claimed invention as a whole, but also to suggest to one of ordinary skill in the art modifications needed to meet all the claim limitations. *Litton Industrial Products, Inc. v. Solid State Systems Corp.*, 755 F.2d 158, 164, 225 USPQ 34, 38 (Fed. Cir. 1985).

The examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references. M.P.E.P. § 70602(j) from *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). Obviousness cannot be established by combining references without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent applicant has done. M.P.E.P. § 2144 from *Ex parte Levengood*, 28 USPQ2d 1300, 1302 (Bd. Pat. App. & Inter. 1993) (emphasis added by M.P.E.P.).

The Examiner rejected original claims 1-24 under 35 U.S.C. § 103(a) as being unpatentable over *Fumer* in view of *Dinallo*. Each of claims 1, 9, and 19 are amended herein to more clearly recite features of their respective claimed inventions.

Claim 1, as amended now recites:

1. A method for representing a root bus of a computer system, comprising:

dynamically generating an object-oriented abstraction corresponding to the root bus referencing one or more methods that may be implemented to obtain and/or generate configuration and resource allocation information *for the root bus and any subordinate busses connected either directly or indirectly to the root bus*; and

registering the methods referenced in the object-oriented abstraction via a data structure stored in memory of the computer system. (Emphasis Added)

In support of the § 103(a) rejection of original claim 1, the Examiner states,

Regarding claim 1, *Furner* et al. disclose a method for representing a root bus, comprising:

creating a globally unique identifier (GUID) for the root bus (bus tag 134, FIG. 1B). *Furner* et al. also disclose peripheral buses are characterized by being connected, directly or indirectly, to the CPU-memory bus through bus controllers that actively manage the communication to the hardware devices on the bus (column 10, lines 13-16). Furthermore, *Furner* et al. disclose an installation information table as shown in FIG. 2E, which implies registering functions. However, *Furner* et al. fail to expressly disclose defining an object-oriented abstraction including methods. Nevertheless, *Furner* et al. do suggest the abstracting into functional modules. Thus, applications could refer to hardware instances in a common manner (column 31, lines 41-51).

Dinallo discloses bridging communication between an object oriented component and a procedural programmed device driver (*Dinallo*, column 2, lines 4-16). As shown in Fig. 3, Object includes multiple methods to provide different functions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of *Furner* et al. to incorporate the teachings of *Dinallo* to obtain the invention as specified in claim 1 because bridging communication between an object oriented component and a procedural programmed device driver the existing procedural programmed device driver could be reused in the OOP environment.

As stated in the Abstract, *Furner* discloses,

An automatic identification system in a computer system having a plurality of hardware instances located on hardware devices in the computer system. The computer system includes a plurality of physical slots each configured to receive a hardware device and referenced by a slot number. The system comprises means for assigning a hardware instance value to each of the plurality of hardware instances, the hardware instance value being unique within the computer system when two or more of the plurality of physical slots are assigned a slot number that is not unique within the computer system. Advantageously, the hardware instance value is unique within the computer system when two or more of the plurality of hardware instances are located on one of the hardware devices or when one or more of the hardware devices is installed in an expansion chassis coupled to the computer system. The hardware instance value is also unique within the computer system when one of the hardware devices includes one or more of the hardware instances coupled to an I/O bus within the hardware device or when one or more of the hardware devices is installed on a system board in the computer system. In one embodiment of the invention, the hardware instance value is a hardware instance number. In another embodiment, the hardware

instance value is a hardware instance name that is easily identifiable by the user.

Furner uses an identification and configuration system 119 to identify hardware devices and hardware instances on those devices. With respect to the Examiner's comment of, "*Furner* et al. disclose an installation information table as shown in FIG. 2E, which implies registering functions," the installation information table stores information related to hardware device drivers. In further detail, *Furner* states,

> As will be explained in detail below, the identification and configuration system 119 of the present invention determines the optimal driver 121 for a particular hardware instance 150 by comparing various characteristics of all the drivers that are capable of supporting the hardware instance. To determine which drivers 121 can support a particular hardware instance, the identification and configuration system 119 compares the information in each driver record 241 with that in the hardware device records 240. *This process identifies drivers 121 that can support the particular hardware instance 150.* (Col 15, lines 8-18, emphasis added)

and

> Once an optimal *driver* 121 is selected, the identification and configuration system 119 places installation information for the selected *driver* into an *installation information table* 133 shown in FIG. 2E. The installation table 133 includes such information as the driver name 207, driver location 208, resource settings 142, and HIN number 222. *The identification and configuration system 119 uses the installation information table 133 to configure the hardware instance 150 in a manner described below.* (Col 15, lines 46-54, emphasis added)

It is clear from above that the installation information table 133 stores information identifying a selected driver for a corresponding hardware instance (*e.g.*, a hardware device driver). Such a driver is employed to access and configure its corresponding hardware instance. *Furner* does not store any information relating to "one or more *methods* that may be implemented to obtain and/or generate configuration and resource allocation information *for the root bus and any subordinate busses connected either directly or indirectly to the root bus*. Under *Furner*, configuration and resource allocation information for root busses and subordinate busses is obtained by the identification and

configuration system 119. There is no method or methods that are registered in memory to perform this operation. The only functions that are registered under *Furner* relate to drivers specific to respective hardware devices and/or hardware instances.

The Examiner further makes reference to Col. 31, lines 40-51, which states,

> There are portions of this identification and configuration system 119 which could be abstracted into functional modules, as in a functional programming language or object-oriented programming language such as C++, such as the automatic identification mechanism 301 and the configuration mechanism 302. These functional modules could be made available to applications such as installation utilities as shown above, monitoring software and network management software *for the purpose of identifying and configuring hardware instances*. Thus, applications could refer to hardware instances in a common manner. (Emphasis added)

The foregoing explicitly states that the functional modules could be employed *for the purpose of identifying and configuring hardware instances*. The one or more methods recited in claim 1 concern methods that are use to obtain and/or generate configuration and resource allocation information *for the root bus and any subordinate busses connected either directly or indirectly to the root bus*. Clearly, the methods referred to in claim 1 serve an entirely different function than the device drivers employed by *Furner* (which conceivably could be accessed via the theoretical functional modules discussed above).

With respect to the Examiner's statement that *Dinallo* discloses bridging communication between an object oriented component and a procedural programmed device driver, the Applicants agree. However, the one or more methods referred to in claim 1 do not relate to device drivers for hardware devices or instances, as discussed above.

In view of the foregoing argument it is clear that the combination of *Furner* and *Dinallo* do not teach or suggest all of the elements and limitations recited in claim 1, as required by the third prong of the *In Re Vaeck* test. Accordingly, a rejection of claim 1, as amended, as being unpatentable over *Furner* in view of *Dinallo* would be

unsupported and thus improper. Accordingly, amended claim 1 is patentable over the cited art.

With respect to amended independent claim 19, this claim is a Beauregard claim reciting software (*i.e.*, computer-executable instructions) for performing operations analogous to the operations recited in amended claim 1. Accordingly, amended claim 19 is patentable over the combination of *Furner* and *Dinallo*.

With respect to amended independent claim 9, this claim recites, in part,

defining an object oriented representation of each root bus comprising a set of components that includes references to *a plurality of methods that may be implemented to obtain and/or generate configuration and resource allocation information for that root bus and any subordinate busses connected either directly or indirectly to the root bus*;

assigning a bus identifier for each of the subordinate busses *through use of an enumeration process that implements one or more of the methods referenced by the object oriented representation of that root bus*; (Emphasis added)

Again, the methods referred to in independent claim 9 are not drivers for hardware devices/instances. Accordingly, it is clear that the combination of *Furner* and *Dinallo* do not teach or suggest all of the elements and limitations recited in claim 1, as required by the third prong of the *In Re Vaeck* test. Accordingly, amended claim 1 is patentable over the cited art.

Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, independent claims 1, 9, and 19 are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 292-8600.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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R. Alan Burnett
Reg. No. 46,149

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030

In the Drawing Figures

Please replace the drawings sheets for FIG. 1 and FIGs. 4, 5A and 5B with the attached replacement sheets. In FIG.1, reference numbers 26 and 28 have been swapped to correspond to the reference numbers recited in the specification. In FIG. 4, original block 70 has been renumbered as block 72, as recited in the specification.

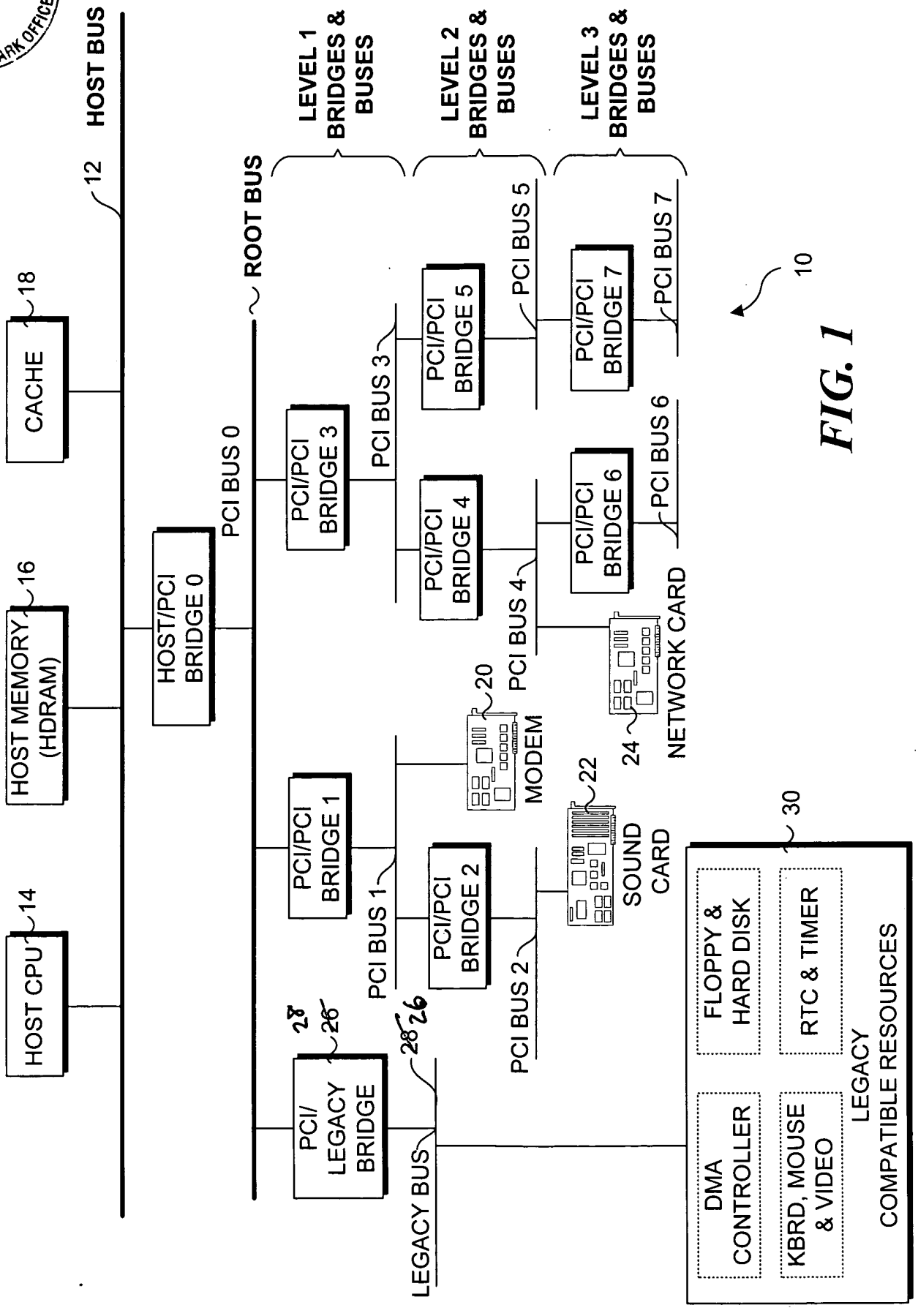

FIG. 1

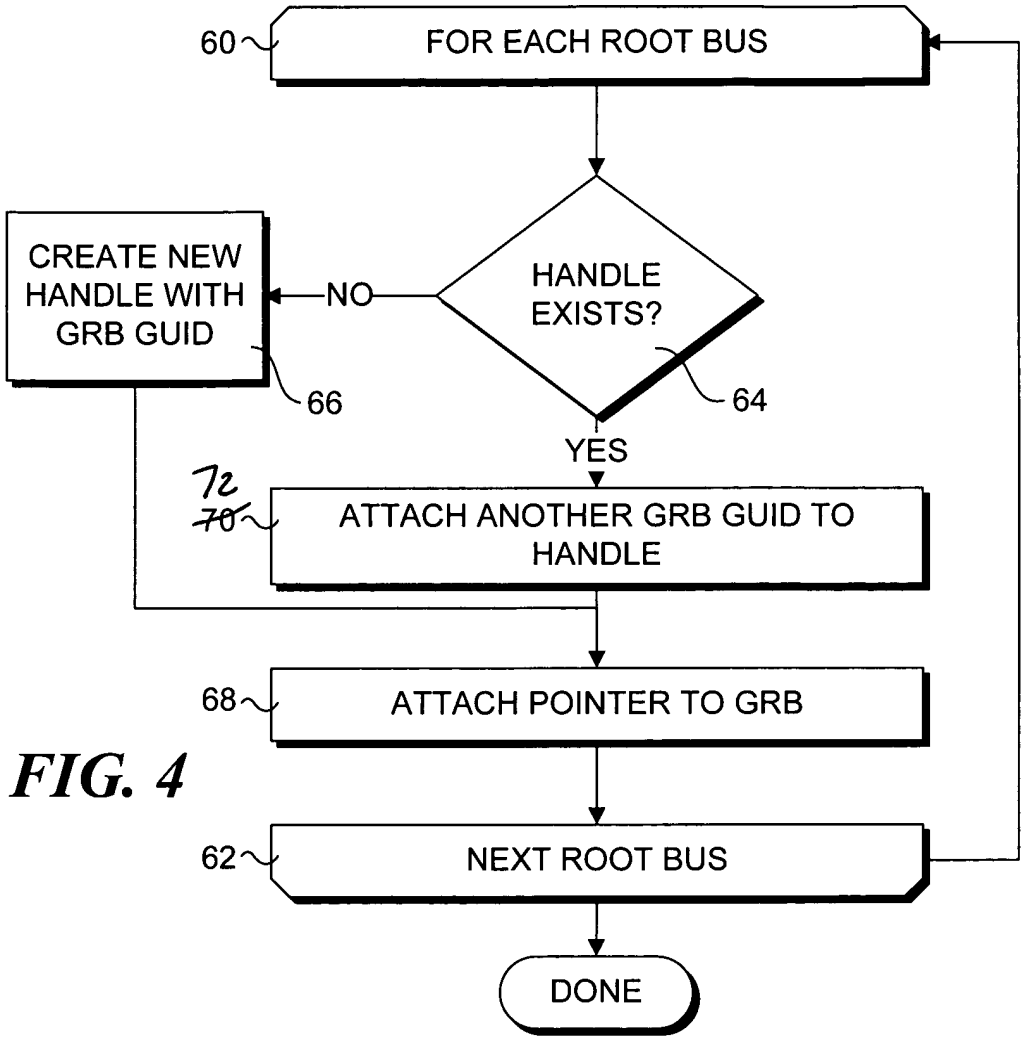

FIG. 4

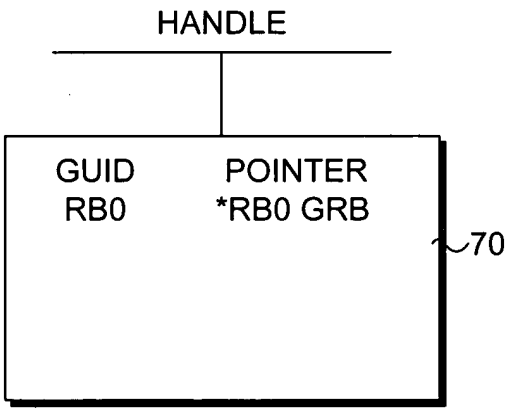

FIG. 5A

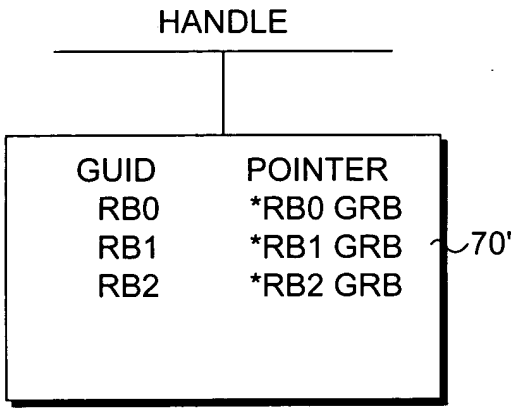

FIG. 5B